## ALTERA方案

### FFT IP CORE信息:

|  |  |
| --- | --- |
| **Name** | altera\_fft\_ii |
| **Version** | 15.1 |
| **Author** | Altera Corporation |
| **Description** | Altera Fast Fourier Transform II |
| **Group** | DSP/Transforms |
| **User Guide** | [https://documentation.altera.com/#/link/hco1419012539637/hco1419012438961](https://documentation.altera.com/%23/link/hco1419012539637/hco1419012438961) |
| **User Guide** | [https://documentation.altera.com/#/link/hco1419012539637/hco1419012438961](https://documentation.altera.com/%23/link/hco1419012539637/hco1419012438961) |
| **Release Notes** | [https://documentation.altera.com/#/link/hco1421698042087/hco1421697815758](https://documentation.altera.com/%23/link/hco1421698042087/hco1421697815758) |
| **Transform** | |
| **Length** | The transform length or the maximum transform length if variable streaming data flow. |
| **Direction** | The direction of the transform. Bi-directional will allow run time control of the transform direction. |
| **I/O** | |
| **Data Flow** | Data flow architectures trade-off throughput and features against resource requirements:  Variable Streaming architecture provides continuous processing of transforms and run time control of the transform length  Streaming architecture provides continuous processing of transforms  Buffered Burst architecture requires fewer memory resource than the streaming architecture at the expense of lower average throughput  Burst architecture requires the fewest memory resources at the expense of the lowest average throughput |
| **Input Order** | The order of the input data |
| **Output Order** | The order of the output data |
| **Data and Twiddle** | |
| **Representation** | Number representation of data and twiddle factors |
| **Data Input Width** | Data input width |
| **Twiddle Width** | Twiddle width |
| **Data Output Width** | Data output width |
| **Latency Estimates** | |
| **Calculation Latency** | Number of cycles the FFT takes to perform the Calculation |
| **Throughput Latency** | Number of cycles from data in to data out |
| **Calculation Latency** | Number of cycles the FFT takes to perform the Calculation |

### 各配置资源评估

下表中结果是基于 Cyclone V 5CEBA4F17A7平台（标红表示与CFG 1#区别），在QuartusII Prime 15.1环境下编译得到

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CFG** | **Transform** | | **I/O** | | | **Data & Twiddle** | | | **Latency** | | **FPGA Resource & Performance** | | | |
| **Length** | **Direction** | **Data Flow** | **Input Order** | **Output Order** | **Representation** | **Data Width** | **Twiddle Width** | **Calculation Latency** | **Throughput Latency** | **ALM** | **DSP** | **M10K** | **Fmax** |
| **1#** | **2048** | **Bi** | **Variable Streaming** | **Natural** | **Bit Reverse** | **Fixed Point** | **16** | **18** | **2048** | **2048** | **2651** | **10** | **20** | **184.77MHz** |
| **2#** | 2048 | Bi | Variable Streaming | Natural | Natural | Fixed Point | 16 | 18 | 2048 | 4096↑ | 2670↑ | 10 | 27↑ | 181.06MHz |
| **3#** | 2048 | Bi | Variable Streaming | Natural | Bit Reverse | Fixed Point | 16 | 16 | 2048 | 2048 | 2620↓ | 10 | 20 | 180.7MHz |
| **4#** | 2048 | Bi | Variable Streaming | Natural | Digit Reverse | Single Floating Point | 16 | 18 | 2048 | 4096↑ | 16138↑ | 24↑ | 167↑ | 165.29MHz |
| **5#** | 2048 | Bi | Streaming | Natural | Natural | Block Floating Point | 16 | 18 | 2048 | 2048 | 2903↑ | 12↑ | 39↑ | 199.16MHz |
| **6#** | 2048 | Bi | Burst Single Output | Natural | Natural | Block Floating Point | 16 | 18 | 6765↑ | 2668↑ | 844↓ | 2↓ | 9↓ | 193.27MHz |

### FFT IP Core配置说明

## XILINX方案

### FFT IP Core信息

### 各配置资源评估：

下表中结果是基于 Artix-7 XC7A100T平台（标红表示与CFG 1#区别），在ISE 14.7环境下编译得到

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CFG** | **Implementation** | **Data Format** | **Precision** | | **Output Ordering** | **Latency** | **Resource** | | | **Performance** |
| **Input** | **Phase Factor** | **Slices** | **BRAM** | **DSP48E1** | **Fmax** |
| 1 | Radix-4, Burst I/O | Fixed Point | 16 | 17 | Natural | 7308 | 582 | 7 | 9 | 228.885MHz |
| 2 | Pipelined, Streaming I/O | Fixed Point | 16 | 17 | Natural | 6296 | 1329 | 11 | 15 | 200.080MHz |
| 3 | Radix-2, Burst I/O | Fixed Point | 16 | 17 | Natural | 15575 | 273 | 5 | 3 | 218.723MHz |
| 4 | Radix-2 Lite, Burst I/O | Fixed Point | 16 | 17 | Natural | 26804 | 243 | 5 | 2 | 216.638MHz |
| 5 | Radix-4, Burst I/O | Floating Point | 32 | 24 | Natural | 9355 | 1178 | 19 | 24 | 207.383MHz |