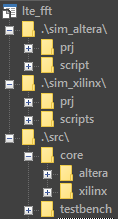
## 文件说明



上图为文件夹总览，共三个文件夹：sim\_altera、sim\_xilinx和src

* sim\_altera文件夹包含prj和script两个子文件夹，prj子文件夹中是QuarutsII的工程文件，script子文件夹中是Modelsim的仿真平台脚本
* sim\_xilinx文件夹包含prj和scripts两个子文件夹，prj子文件夹中是ISE的工程文件，scripts文件夹中是仿真Modelsim的仿真平台脚本
* src文件夹，根目录包含源代码LTE\_FFT.v、preproc.v、postproc.v和lte\_fft\_inc.v；core子文件夹中包含altera和xilinx FFT IP core的源码；testbench子文件夹中包含仿真testbench源码

## 系统结构

LTE\_FFT的FPGA实现结构如下图所示，数据流走向： preproc 🡪 FFT/IFFT 🡪 postproc

**preproc**模块用于在FFT模式下，去除CP，将有用数据缓存在乒乓RAM中，引入乒乓RAM结构是为了在写入数据的同时能读取数据；而在IFFT模式下，数据不做缓存直接引入IFFT中。

**postproc**模块用于在IFFT模式下，先将有用数据缓存在乒乓RAM中，然后读取并插入CP数据；而在FFT模式下，数据不做缓存直接输出。



## ALTERA方案

### FFT IP CORE信息:

|  |  |
| --- | --- |
| Name | altera\_fft\_ii |
| Version | 15.1 |
| Author | Altera Corporation |
| Description | Altera Fast Fourier Transform II |
| Group | DSP/Transforms |
| User Guide | [https://documentation.altera.com/#/link/hco1419012539637/hco1419012438961](https://documentation.altera.com/%23/link/hco1419012539637/hco1419012438961) |
| User Guide | [https://documentation.altera.com/#/link/hco1419012539637/hco1419012438961](https://documentation.altera.com/%23/link/hco1419012539637/hco1419012438961) |
| Release Notes | [https://documentation.altera.com/#/link/hco1421698042087/hco1421697815758](https://documentation.altera.com/%23/link/hco1421698042087/hco1421697815758) |
| Transform | |
| Length | The transform length or the maximum transform length if variable streaming data flow. |
| Direction | The direction of the transform. Bi-directional will allow run time control of the transform direction. |
| I/O | |
| Data Flow | Data flow architectures trade-off throughput and features against resource requirements:  Variable Streaming architecture provides continuous processing of transforms and run time control of the transform length  Streaming architecture provides continuous processing of transforms  Buffered Burst architecture requires fewer memory resource than the streaming architecture at the expense of lower average throughput  Burst architecture requires the fewest memory resources at the expense of the lowest average throughput |
| Input Order | The order of the input data |
| Output Order | The order of the output data |
| Data and Twiddle | |
| Representation | Number representation of data and twiddle factors |
| Data Input Width | Data input width |
| Twiddle Width | Twiddle width |
| Data Output Width | Data output width |
| Latency Estimates | |
| Calculation Latency | Number of cycles the FFT takes to perform the Calculation |
| Throughput Latency | Number of cycles from data in to data out |
| Calculation Latency | Number of cycles the FFT takes to perform the Calculation |

### 各配置资源评估

下表中结果是基于 Cyclone V 5CEBA4F17A7平台（标红表示与CFG 1#区别），在QuartusII Prime 15.1环境下编译得到，FFT长度2048点

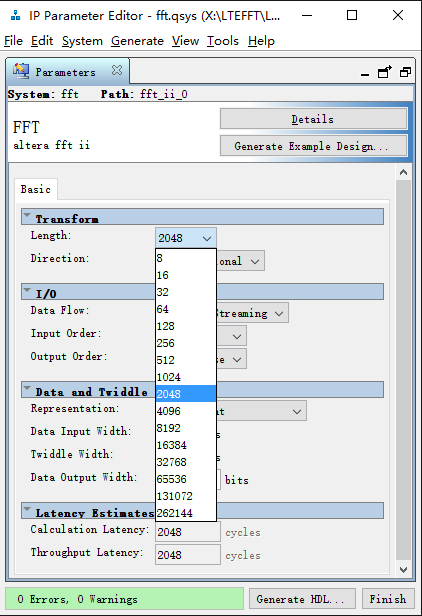
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| CFG | I/O | | | Data & Twiddle | | | Latency | | FPGA Resource & Performance | | | |
| Data Flow | Input Order | Output Order | Representation | Data Width | Twiddle Width | Calculation Latency | Throughput Latency | ALM  10Kb | DSP  18X18 | M10K | Fmax |
| 1 | Variable Streaming | Natural | Natural | Fixed Point | 16 | 18 | 2048 | 4096 | 2670 | 10 | 27 | 181.06MHz |
| 2 | Variable Streaming | Natural | Bit Reverse | Fixed Point | 16 | 18 | 2048 | 2048↓ | 2651↓ | 10 | 20↓ | 184.77MHz |
| 3 | Variable Streaming | Natural | Bit Reverse | Fixed Point | 16 | 16 | 2048 | 2048↓ | 2620↓ | 10 | 20 | 180.7MHz |
| 4 | Variable Streaming | Natural | Digit Reverse | Single Floating Point | 16 | 18 | 2048 | 4096 | 16138↑ | 24↑ | 167↑ | 165.29MHz |
| 5 | Streaming | Natural | Natural | Block Floating Point | 16 | 18 | 2048 | 2048↓ | 2903↑ | 12↑ | 39↑ | 199.16MHz |
| 6 | Burst Single Output | Natural | Natural | Block Floating Point | 16 | 18 | 6765↑ | 2668↓ | 844↓ | 2↓ | 9↓ | 193.27MHz |

注：资源方面，CFG 6方案最少，但是采用的是Block Floating Point处理，剩余的CFG 1、CFG 2都相差无几；CFG 1相比CFG2多7个M10K块，区别是输出数据顺序，在外部实现数据顺序翻转也需要消耗近7个M10K块，因此最终选择CFG 1方案。

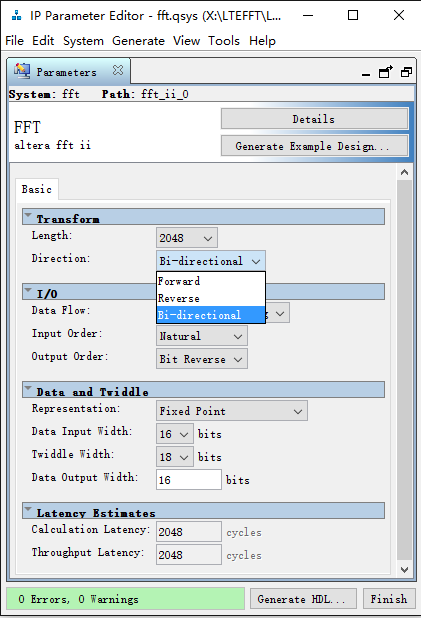
### FFT IP Core配置说明

软件环境：QuartusII Prime 15.1

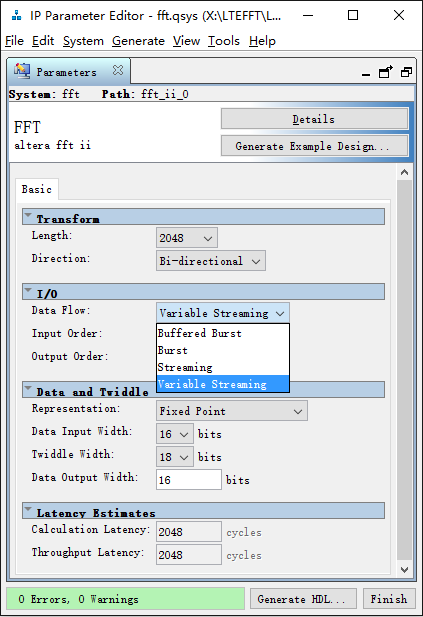
* 在**Transform -- Length**中设置FFT点数，选择2048



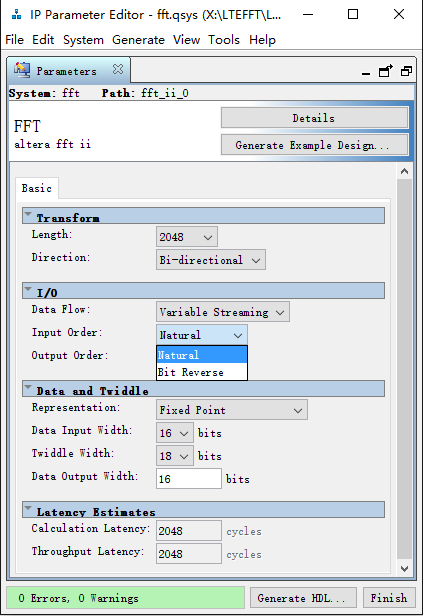
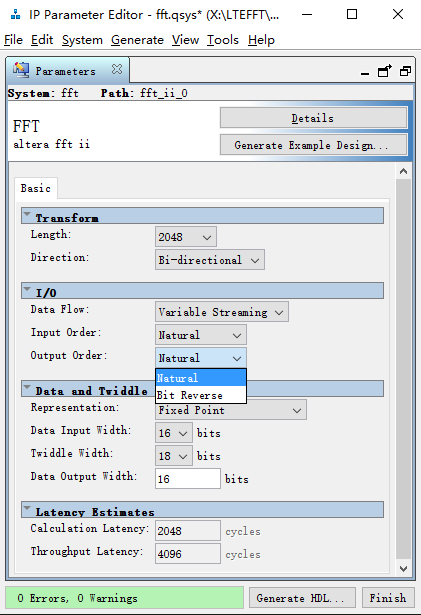
* 在**Transform -- Direction**中设置FFT变换方向，设置**Bi-directional**，可随时切换FFT变换方向



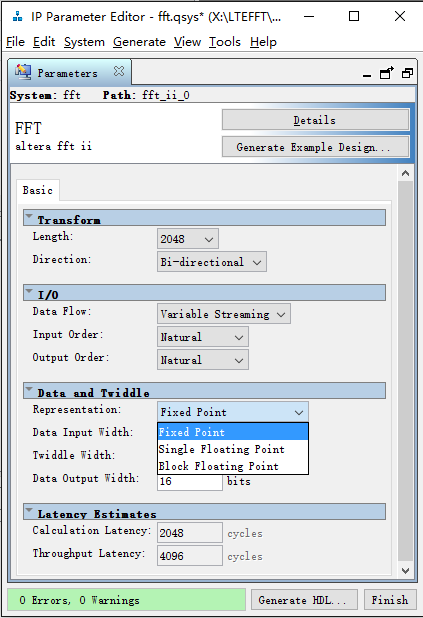
* 在**I/O – Data Flow**中设置数据数据模式，设置**Variable Streaming**，可随时改变FFT点数，其中Length设置的2048点是最大点数



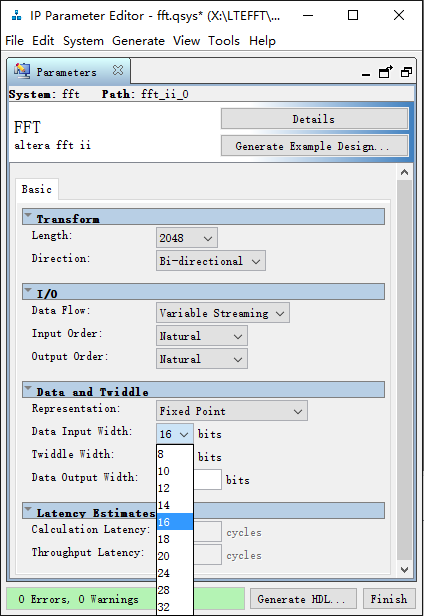
* 在**I/O – Input Order**和**Output Order**中，设置数据输入顺序，**Input Order**设置为**Natural**，**Output Order**设置为**Natural**

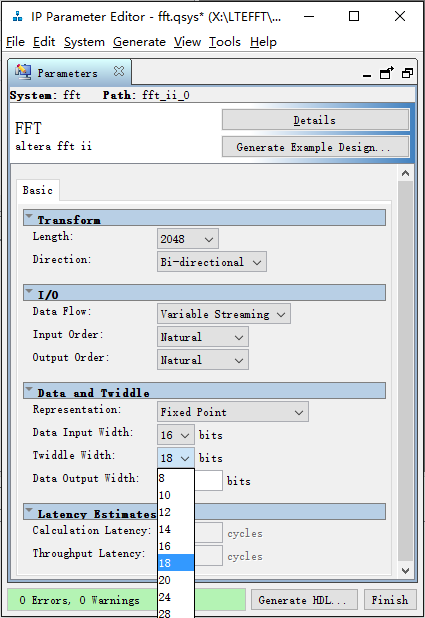
* 在**Data and Twiddle – Representation**中设置数据处理类型，设置为Fixed Point，定点性



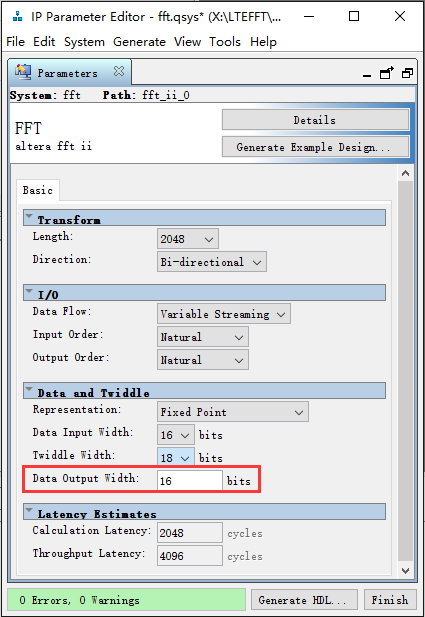
* 在**Data and Twiddle – Data Input Width**中设置输入数据的位宽，设置值必须与LTE\_FFT.v中参数BIT\_WIDTH的值一致



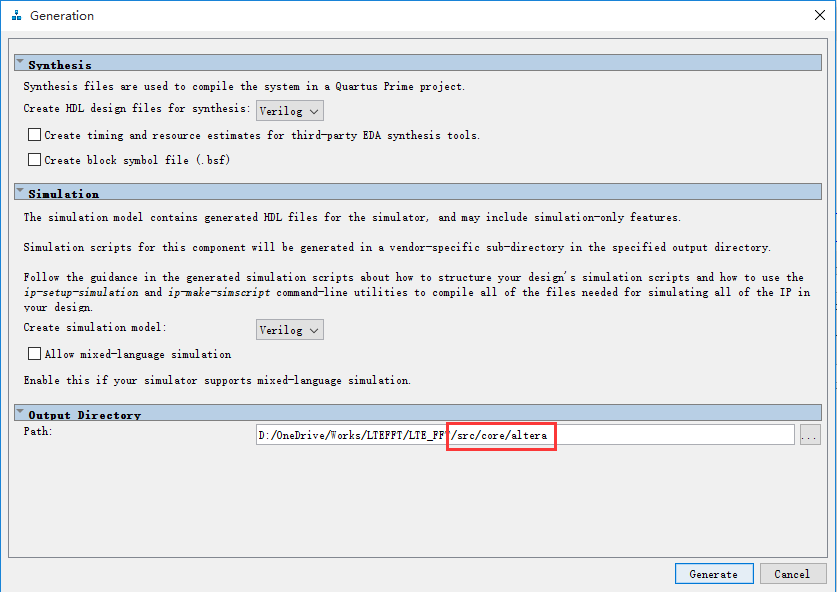
* 在**Data and Twiddle – Twiddle Width**中设置旋转因子数据的位宽，Cyclone V中DSP模块支持18X18的乘法，因此设置为18



* 在**Data and Twiddle -- Data Output Width**设置输出数据的位宽，设置与**Data Input Width**保持一致



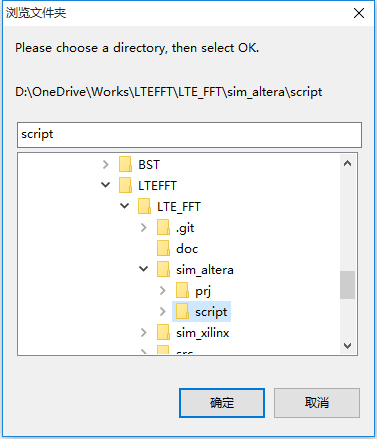
* 点击**Generate HDL**生成用于综合和仿真的源码，需要将路径设置到 **.\src\core\altera** 文件夹中



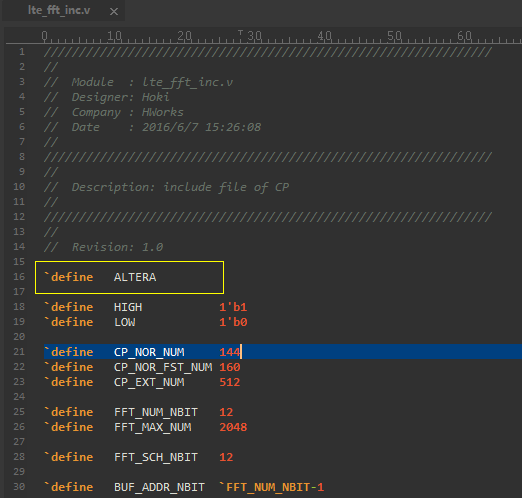
### 仿真平台

仿真平台在Modelsim/QuestaSim中执行，流程如下

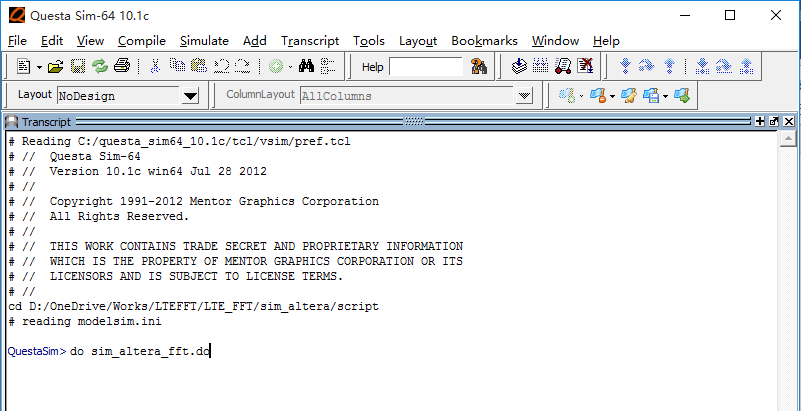
* 选择**File – Change Directory**，切换当前路径到.\sim\_altera\script\文件夹



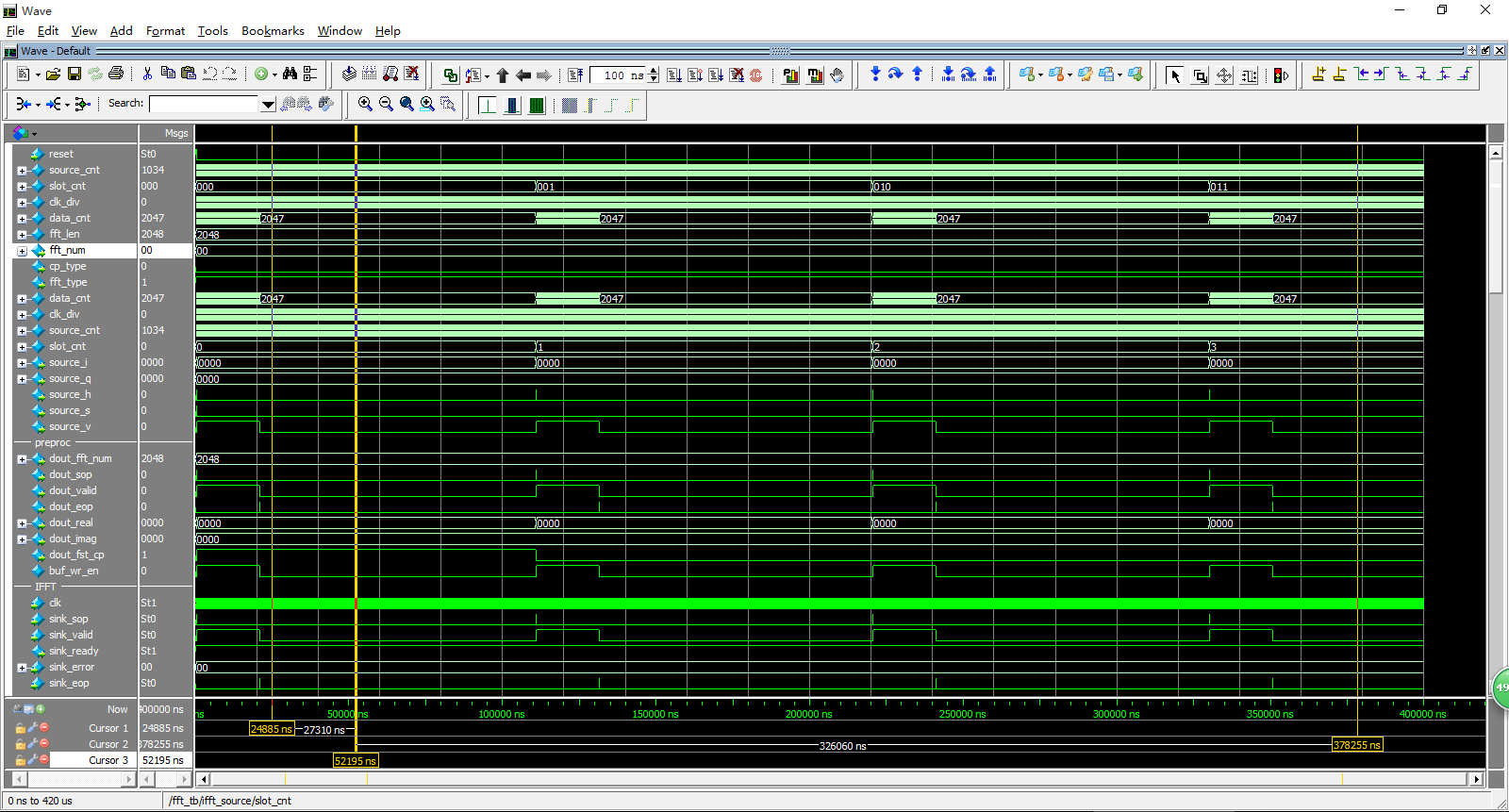
* 修改src文件夹中的lte\_fft\_inc.v文件，加入`define ALTERA宏定义代码，这样仿真器可识别此次仿真时针对Altera 的IP Core



* 在命令行窗口输入: do sim\_altera\_fft.do，开始自动编译库、编译代码和仿真



* 仿真时会自动加载wave波形窗口，可观察所有内部信号时序



## XILINX方案

### FFT IP Core信息

Xilinx Fast Fourier Transform (FFT) ，版本7.0，基于Cooley-Tukey FFT算法。

### 各配置资源评估：

下表中结果是基于 Artix-7 XC7A100T平台（标红表示与CFG 1#区别），在ISE 14.7环境下编译得到

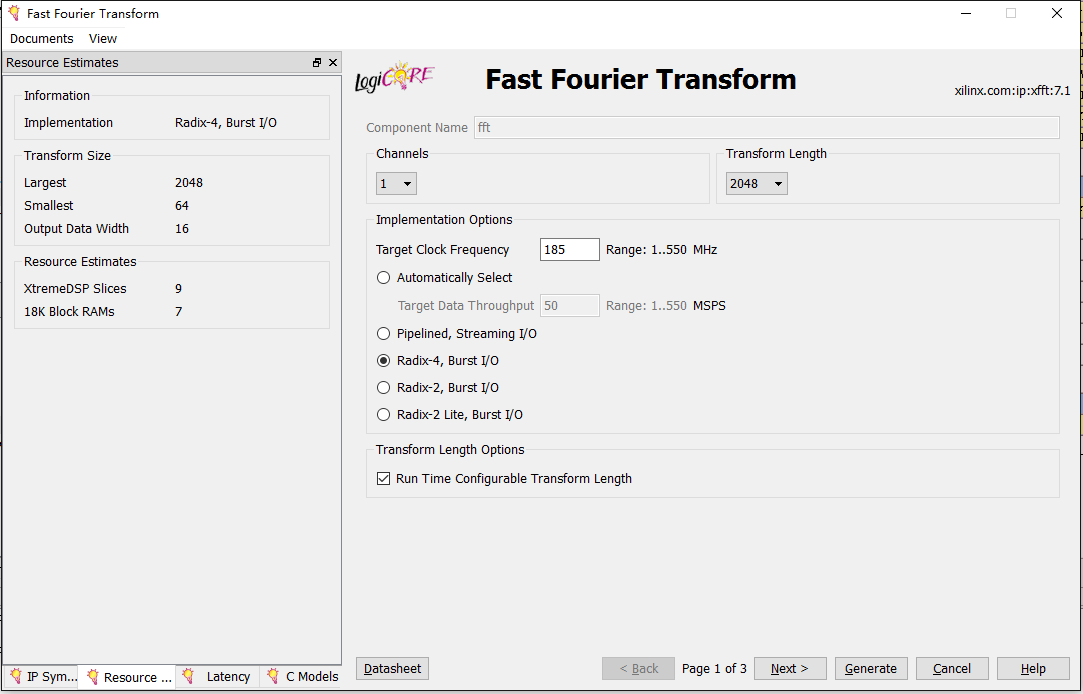
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **CFG** | **Implementation** | **Data Format** | **Precision** | | **Output Ordering** | **Latency** | **Resource** | | | **Performance** |
| **Input** | **Phase Factor** | **Slices** | **BRAM**  **18kb** | **DSP48E1**  **18X18** | **Fmax** |
| 1 | Radix-4, Burst I/O | Fixed Point | 16 | 17 | Natural | 7308 | 582 | 7 | 9 | 228.885MHz |
| 2 | Pipelined, Streaming I/O | Fixed Point | 16 | 17 | Natural | 6296↓ | 1329 | 11↑ | 15↑ | 200.080MHz |
| 3 | Radix-2, Burst I/O | Fixed Point | 16 | 17 | Natural | 15575↑ | 273↓ | 5↓ | 3↓ | 218.723MHz |
| 4 | Radix-2 Lite, Burst I/O | Fixed Point | 16 | 17 | Natural | 26804↑ | 243↓ | 5↓ | 2↓ | 216.638MHz |
| 5 | Radix-4, Burst I/O | Floating Point | 32 | 24 | Natural | 9355↑ | 1178↑ | 19↑ | 24↑ | 207.383MHz |

注：资源方面，CFG 3消耗最少，但是性能不达标，延时15575个时钟周期，而系统所允许的最大延时为(CLK\_FS\_RATIO-1)\*2048 = 8192，满足要求的只有CFG 1和CFG 2，相比下，最终选择资源少的CFG 1方案： Radix-4 Burst I/O

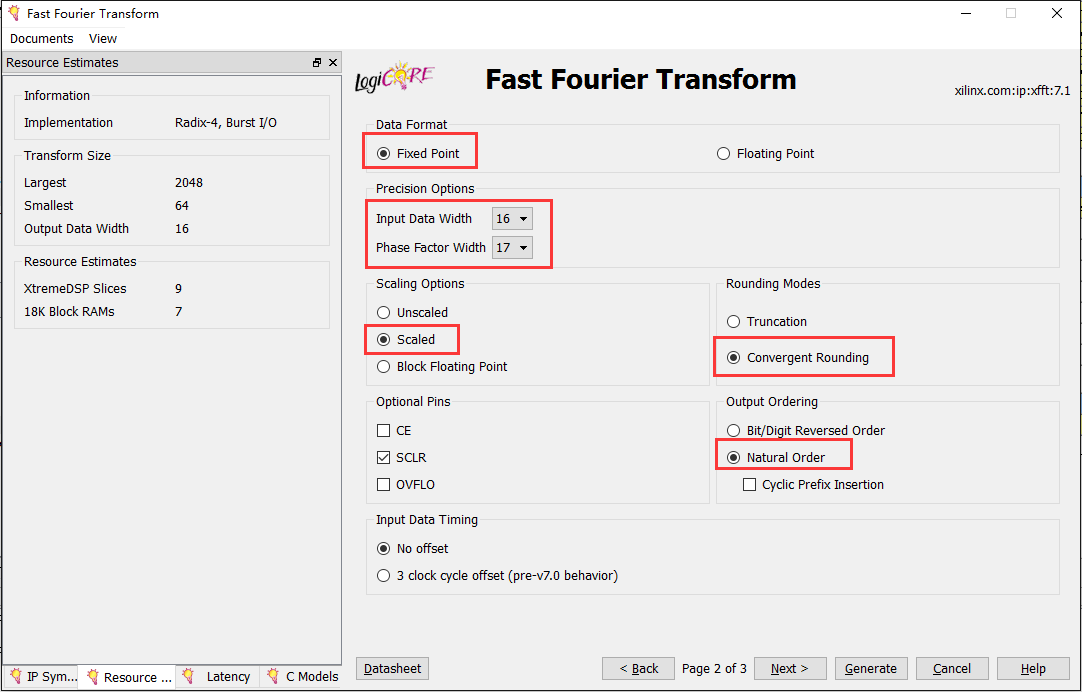
### FFT IP Core配置说明

软件环境：ISE Project Navigator 14.7

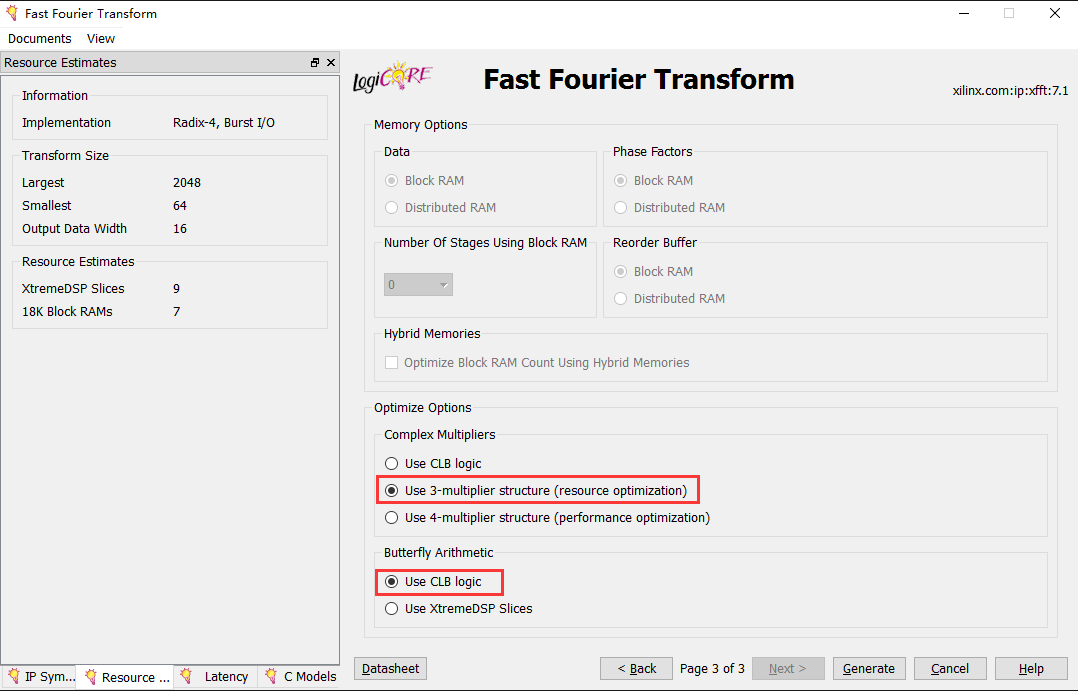
* 配置Page 1页：Channels 设置1；Transform Length设置2048；Implementation Options设置Radix-4, Burst I/O；Transform Length Options勾选Run Time Configurable Transform Length



* 配置Page 2页：Data Format选择Fixed Point；Precision Option中设置Input Data Width与LTE\_FFT.v的参数一致，Phase Factor Width设置17；Scaling Options设置Scaled，保证输出数据与输入数据的位宽一致；Rounding Modes选择Convergent Rounding，减少数据截取直流分量的引入；Output Ordering选择Natural Order



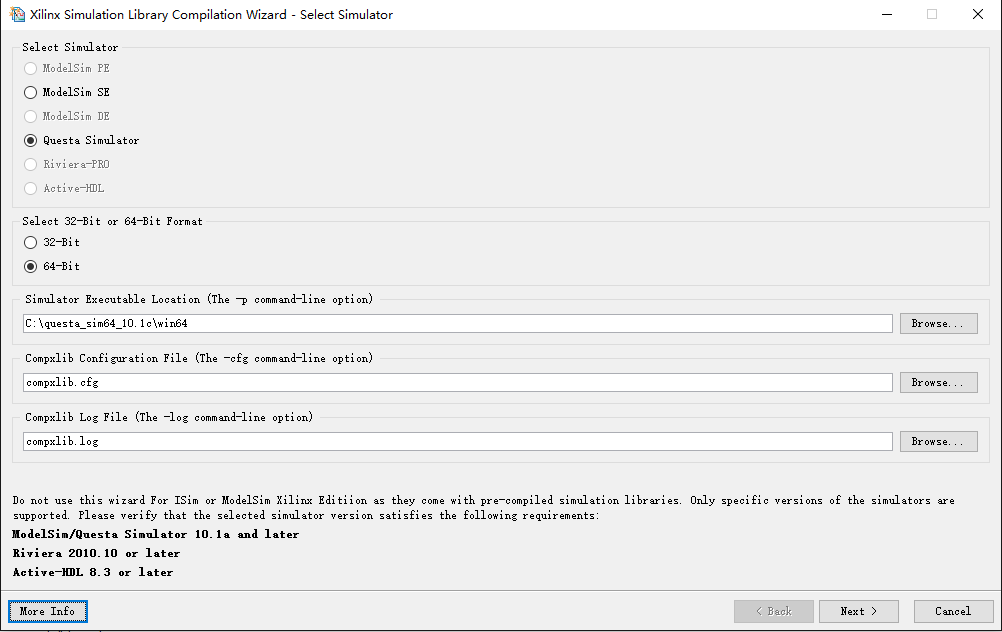
* 配置Page 3页：Complex Multipliers选择Use 3-multiplier structure；Butterfly Arithmetic选择Use CLB logic；两个选项都倾向于资源优化方向



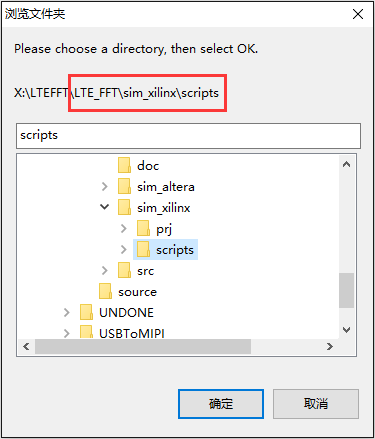
### 仿真平台

仿真平台在Modelsim/QuestaSim中执行，流程如下

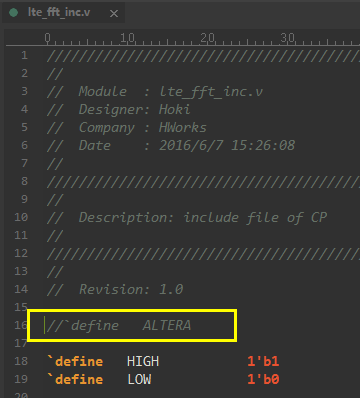
* Modelsim/QuestaSim中提前编译Xilinx仿真库，可使用ISE软件自带工具Simulation Library Compilation（Altera方案仿真平台无需此步骤）



* 选择**File – Change Directory**，切换当前路径到.\sim\_xilinx\scripts\文件夹



* 在lte\_fft\_inc.v中取消ALTERA宏定义



* 在命令行窗口输入: do sim\_xilinx\_fft.do，开始自动编译库、编译代码和仿真

